ERRATA

Rev. 3.1 (1/1)

MP8931A Operation Manual

The following revisions were made after the third edition of the MP8931A Operation Manual was issued. Please read the column on the right for the changes to the items in the column on the left.

PAGE	FOR	READ
P. A-2	Appendix A Specifications (2)NRZ/External clock input interface Output signal Data Tr/Tf(20 to 80%) 1 ns or less(ECL)	Tr/Tf(20 to 80%) 1 ns or less(ECL), 1.5 ns or less(TTL)
	Appendix A Specifications (2)NRZ/External clock input interface Output signal Clock Tr/Tf(20 to 80%) 1 ns or less(ECL)	Tr/Tf(20 to 80%) 1 ns or less(ECL), 1.5 ns or less(TTL)
	Output phase | t | ≦ 1ns(at ECL level)	Output phase | t | ≦ 1ns(at ECL level) | t | ≦ 2ns(at TTL level)
P. A-4	Appendix A Specifications (3)DVB-SPI interface Output signal Common to Clock, Data DVALID, PSYNC Level(LVDS) Offset Voltage :1.1 to 1.35V Differential Output Voltage : 250 to 450mv	Level(LVDS) Offset Voltage :1.125 to 1.35V Differential Output Voltage : 247 to 454mv